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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,477	09/29/2003	Goichi Ono	NITT.0156	1514
38327	7590	06/29/2004	EXAMINER	
REED SMITH LLP 3110 FAIRVIEW PARK DRIVE, SUITE 1400 FALLS CHURCH, VA 22042			ENGLUND, TERRY LEE	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/671,477

Applicant(s)

ONO ET AL.

Examiner

Terry L England

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on Interview (Jun 23, 2004).
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 September 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☒ Certified copies of the priority documents have been received in Application No. 10/284,207.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>09232003</u> | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Priority***

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 10/284,207, filed on Oct 31, 2002.

### ***Drawings***

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Fig. 13 "135" is not described in the specification. Instead, "35" is described (e.g. see page 19, lines 17, 20, and 23; and page 20, line 13). Therefore, it is suggested Fig. 13's "135" be changed to -- 35-- in order to correspond to the figure's description, or the disclosure's "35" will have to be changed to --135--.. Corrected drawing sheets, or amendment to the specification to add the reference character(s) in the description, are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to because Fig. 12 shows 123 receiving "vban" instead of "vbap" as described on page 19, line 9. [It is noted that Fig. 13 of the present application, and corresponding Figs. 12-13 of parent application 10/284,207, clearly show 123 receiving "vbap."]

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Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Note: When corrected drawings are submitted, it is suggested Fig. 6 show shift register 24 clearly receiving signals "up" and "down" as described on page 13, lines 26-27. However, this change is neither necessary nor critical, and odes not have to be made.

### *Specification*

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. For example, wording such as --Well bias voltage control circuit and method-- describes the invention more clearly than the present generic "Semiconductor integrated circuit device" title.

The abstract of the disclosure is objected to because several of the reference designators (i.e. "13" and "15") are not clearly identified within the figures. Therefore, unless all reference

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designators are removed from the abstract, the following changes are suggested to ensure the abstract's description corresponds to what is shown within the figures (e.g. Fig. 2): "monitor 11" on lines 3, 7 and 8 (two occurrences) should be --monitor 21--; and "circuit 13" on line 5 and "circuit 15" on line 7 should both be --circuit 23--. Since "by a CMOS" on lines 3 and 4 is vague, it is suggested that phrase be changed to --with a CMOS device--. It is also suggested "Disclosed is a" on line 1 be changed to simply --A-- because it is understood the abstract should be describing/summarizing what is disclosed. Corrections are required. See MPEP § 608.01(b).

The disclosure is objected to because of the following informalities: The newly added paragraph identifying the continuation and priority applications should be updated to indicate parent application 10/284,207 was issued on Nov 25, 2003 as U.S. Patent 6,653,890. Page 20, line 21 "23" should be --123-- because the description is about the second embodiment (related to Figs. 12 and 13). Also, line 27 on the same page clearly identifies the circuit as "123." Appropriate corrections are required.

### ***Claim Objections***

Claims 2, 3, 6, and 8-14 are objected to because of the following informalities: For consistent labeling, it is suggested --first-- be added prior to "logical" on line 7 of claim 2. Claim 3, line 3 "output" should be --outputs-- to improve word flow. Claim 6, line 3 "first signal" should be --first control signal-- for consistent labeling. Since lines 2-3 of claim 8 already identify the first and second conductivity types, it is suggested the related "a first" and "a second" on respective lines 5, 10, and 11 be changed to --the first-- and --the second-- to clearly relate the conductivity types back to those on lines 2-3. Claim 14, line 6 "monitor signal" should be --monitor circuit-- to correspond to the circuit recited on line 4 of claim 8. Dependent claims

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carry over any objection(s) from any claim(s) upon which they depend. Appropriate corrections are required.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2-5, and 8-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. It is not clear how “a comparator” in claims 2 (line 7) and 4 (line 5) relate to the “comparator” already recited within claim 1. If the applicants’ intend to mean a different comparator, it is suggested “a comparator” in claims 2 and 4 be changed to either --a second comparator-- or --another comparator--. If those changes are made, then corresponding changes must be made with respect to “the comparator” recited on line 2 of both claims 3 and 5. It is not understood if claim 4 has all of its intended limitations recited because the claim lacks the term --and-- which would help identify the last limitation. If the “different detector” is the last limitation, then it is suggested --and-- be added after “signal,” on line 9 of claim 4. It is not understood how “a first well bias voltage” and “a second well bias voltage” on respective lines 14 and 15 of claim 8 relate to the single “a well bias voltage” recited on line 1 of the same claim. If the applicants’ intend to mean the phrases relate to the same voltages within claim 8, it is suggested “a well bias voltage” on line 1 be changed to --first and second well bias voltages--; “a first” on line 14 be changed to --the first--; and “a second” on line 15 be changed to --the second--. If the “a well bias voltage” phrase of claim 8 is modified as suggested above, then the same phrase within line 1 of each of claims 9-14 require the same change. Similar to

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claims 2 and 4 above, it is not clear how "a comparator" in claims 9 (line 8), and 11 (line 7) relate to "a comparator" cited on line 7 of claim 8. If "a comparator" in claims 9 and 11 is changed, then "the comparator" in claims 9 (line 9) and 11 (line 8) needs a corresponding change.

Dependent claims carry over any rejection(s) from any claim(s) upon which they depend.

### ***Double Patenting***

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Apparatus claims 1-7, and an understanding of method claims 8-14, are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over at least independent claim 1 of U.S. Patent No. 6,653,890. Although the conflicting claims are not identical, they are not patentably distinct from each other because the present application's claims recite specific limitations (e.g. in structure or functional steps) that are related to the patent's claimed main circuit (with PMOS and CMOS transistors), and control circuit (with several different means). Therefore, one of ordinary skill in the art would understand additional dependent claims within the patent could have described the various circuits or means in detail, or method claims could have been recited describing the various operational steps. Referring the

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patent's claim 1 limitations to both the present application's figures and the patent's figures, one of ordinary skill in the art would know the lower CMOS inverter within MAIN CIRCUIT 10 of Fig. 1 corresponds to the claimed "main circuit constructed mainly by a CMOS formed by PMOS and NMOS transistors", while CONTROL CIRCUIT 11 corresponds to the "control circuit for controlling a well bias." Fig. 2 shows the control circuit in more detail, wherein it has means 21,22,24,25 for detecting a deviation of delay time and determining well bias  $v_{bap}$ ,  $v_{ban}$  in accordance with the deviation. The control circuit also has means 23 (shown in more detail in Figs. 3 and 4) for detecting a difference threshold between threshold voltages of PMOS and NMOS transistors (e.g. see Fig. 4). Therefore, it is understood that the control circuit corrects well bias  $v_{bap}$ ,  $v_{ban}$  in accordance with the difference by using means 23 and means 21,22,24, 25. Now referring to the present application's claim 1, the first circuit comprises first/second MOS transistors of first/second conductivity types corresponding to the CMOS inverter of the MAIN CIRCUIT shown in Fig. 1. The claimed delay monitor circuit, comparator, well bias voltage generator, and compensation circuit are all considered part of CONTROL CIRCUIT 11, with more specific details shown in other related figures. For example, delay monitor circuit 21 of Fig. 2 can comprise the PMOS/NMOS transistors within the series coupled CMOS inverters shown in Fig. 1, wherein the PMOS and NMOS transistors can be deemed the third and fourth MOS transistors of the first and second conductivity types, respectively. Fig. 2's delay monitor circuit 21 is shown outputting DELAY SIGNAL. Comparator 22 (or 22,24) compares DELAY SIGNAL and CLOCK SIGNAL, and outputs first/second control signals up/down (or  $adrp/adrn$ ). Well bias generator 25 outputs first/second well bias voltages  $v_{bap}$ / $v_{ban}$  to their respective PMOS/NMOS transistors. Compensation circuit 23 is shown in more detail in Figs. 3 and 4,



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wherein it comprises fifth/sixth MOS transistors 41/42 (see Fig. 4) of the first/second conductivity types. Difference signal diff, output by compensation circuit 23 (e.g. see Figs. 2 and 3), is based on the threshold difference vlog of fifth/sixth MOS transistors 41/42. From Figs. 2 and 6, one of ordinary skill in the art would understand first well bias voltage vbap is controlled by first control signal up (or adrp) and second well bias voltage vban is controlled by second control signal down (or adrn) adjusted by difference signal diff. Therefore, the present application's claims cite details one of ordinary skill in the art could relate to the claimed limitations recited in the patent's claim, wherein the present application's dependent claims recite even more specific details. For example, the compensation circuit of claim 2 corresponds to compensation circuit 23 shown in Figs. 2 and 3, with Figs. 3-4 showing more details. The first CMOS inverter of claim 2 comprises fifth/sixth MOS transistors 41/42 (of Fig. 4) outputting first logical threshold voltage vlog. Fig. 3 shows the other components and signals recited within claim 2, wherein reference voltage generator 32 outputs first/second reference signals refa/refb; comparator 33 compares first logical threshold voltage vlog with the first/second reference voltages, and outputs first/second signals up/down; and difference detector 34 detects the difference between the first/second signals, and outputs difference signal diff. Also, one of ordinary skill in the art would know that method claims 8-14 of the present application cite steps, corresponding to the various components recited within the application's apparatus claim(s), which in turn corresponds to the main circuit and control circuit of at least the patent's claim 1.

***Allowable Subject Matter***

No claim is allowable as presently written. However, if the objections and rejections described above are all addressed/corrected satisfactorily, claims 1-14 would be allowable. There is no

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motivation to modify or combine any prior art reference(s) to ensure the device (or method) outputs the first/second well bias voltages as recited within both independent apparatus claim 1 and method claim 8, wherein the first well bias voltage is controlled by the first control signal, and the second well bias voltage is controlled by the second control signal that is adjusted by the difference signal.

***Prior Art***

The prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claimed invention. All three references clearly show and disclose circuitry and/or methods for controlling the well bias voltages applied to MOS transistors of the first and second conductivity types. However, none of these references clearly show or disclose the first well bias voltage controlled by the first control signal, and the second well bias voltage controlled by the second control signal that is adjusted by the difference signal as recited within both independent apparatus claim 1 and method claim 8.

The prior art references cited on the IDS submitted on Feb 9, 2004 were carefully reviewed and considered. [These references were all previously cited with respect to parent application 10/284,207.] For the same reasons as described above, none of these references clearly show or disclose the control and/or adjustment of the first and second well bias voltages as recited within both independent apparatus claim 1 and method claim 8.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

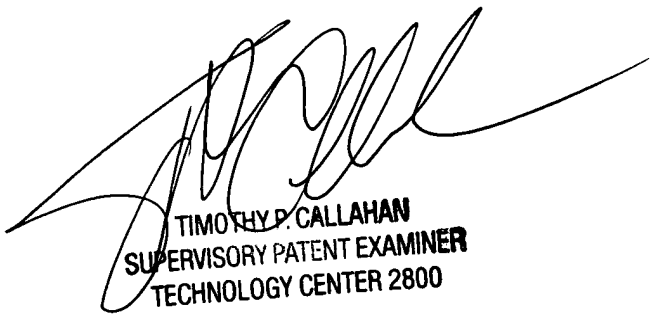
The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

*TLE*

Terry L. Englund

23 June 2004



TIMOTHY P. CALLAHAN  
SUPERVISORY PATENT EXAMINER  
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